02-07-00

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	P00,0184
First Named Inventor or Application Identifier	
Rainald Sander	
Express Mail Label No: #EL393830139US	

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, DC 20231

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Specification [Total Pages 11]
2. X Drawing(s) (35USC 113) [Total Pages 3]
3. X Declaration and Power of Attorney [Total Pages 2]

a. __ Newly executed declaration (Original copy)

b. __ Copy from prior application (37CFR 1.63(d))
(for continuation/divisional with Box 14 completed)

[Note Box 4 Below]
i. __ DELETION OF INVENTOR(S)
Signed statement attached deleting Inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

4. __ Incorporation By Reference (usable if Box 3b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ACCOMPANYING APPLICATION PARTS

5. __ Assignment Papers (cover sheet & documentation)
_____

6. X Letter under 37 CFR 1.41(c).

7. __ English Translation Document *(if applicable)*

8. X Information Disclosure Statement (IDS)/PTO-1449 X Copies of IDS Citations

9. __ Preliminary Amendment

10. X Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

11. __ Small Entity Statement(s) __ Statement filed in prior application, Status still proper and desired

12. __ Certified Copy of Priority Document(s) German Application No. 199 04 575.5 filed February 4, 1999

13. ___ Other:

14. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*

__ Continuation __ Divisional __ Continuation-in-part (CIP) __ of prior application No: /

CLAIMS AS FILED				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) BASIC FEE $690.00
TOTAL CLAIMS 20	9			
INDEPENDENT CLAIMS 3	1			
	ANY MULTIPLE DEPENDENT CLAIMS? ()YES (X) NO			
			TOTAL FILING FEE ->	$690.00

X The Commissioner is hereby authorized to charge any additional fees which may be required in connection with this application, or credit any overpayment to ACCOUNT NO. 08-2290. A duplicate copy of this sheet is enclosed.

X A check in the amount of $ 690.00 to cover the filing fee is enclosed.

15. CORRESPONDENCE ADDRESS

HILL & SIMPSON
A Professional Corporation
233 South Wacker Drive - 85th Floor Sears Tower
Chicago, Illinois 60606
Telephone (312) 876-0200 - Fax (312) 876-0898

SIGNATURE: _____

DATE: February 4, 2000

491/1235:1190
U-11

SPECIFICATION

TITLE

TEMPERATURE-PROTECTED SEMICONDUCTOR SWITCH

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention is directed to a temperature-protected semiconductor switch having a semiconductor switch element which is composed of a number of cells connected in parallel and which includes an integrated reverse diode. The temperature-protected semiconductor switch also has a temperature sensor wherein the semiconductor switch element and the temperature sensor are integrated together in a semiconductor body of a first conductivity type and wherein the temperature sensor generates a first signal given the occurrence of an excessive temperature.

Description of the Prior Art

For protection against thermal overload, semiconductor switches, particularly power switches, are provided with integrated temperature sensors. The temperature sensors acquire the temperature of the power switch and convert this into a temperature-dependent, analog signal which then can be interpreted in a circuit. As a result thereof, for example, a shut-off of the semiconductor switch is possible when a specific, predetermined temperature has been exceeded.

Figure 1a shows a schematic view of such a semiconductor switch. The semiconductor switch 1 is thereby composed of a semiconductor switch element T1, for example a MOSFET, that includes a number of cells (not shown) connected in parallel. A temperature sensor TS is integrated in the proximity of the hottest location; this being potentially implemented, for example, as a diode, a bipolar transistor or, on the other hand, as a thyristor. The temperature sensor TS together with the semiconductor switch element T1 is integrated in a semiconductor body. Via a signal line SL1, the temperature sensor TS outputs a signal when a predetermined temperature is upwardly exceeded, this signal being

processed by an evaluation unit (not shown). The signal then can be taken to shut the semiconductor switch element T1 off. As a result, an overheating and, thus, a destruction of the semiconductor switch element T1 can be avoided. Figure 1b shows the schematic circuit diagram of the semiconductor switch element T1, a MOSFET, and of the temperature sensor TS. Due to technology, a MOSFET includes an integrated reverse diode D1. Many versions are known for the interconnection of a temperature sensor TS with the semiconductor switch element so that only a block symbol is shown for the temperature sensor; this being connected to a status output ST1 via the signal line 1. A circuit arrangement for acquiring the excess temperature of a semiconductor switch in integrated form is disclosed, for example, by EP 0 341 482 A1.

When the temperature sensor together with the semiconductor switch element is integrated in a semiconductor body, the technologically integrated diode can present problems for the semiconductor switch element from source to drain. When this is operated statically or temporarily in flow direction, it produces free charge carriers. The free charge carriers form a parasitic structure together with the integrated temperature sensor. This can lead to the fact that the temperature sensor assumes it has detected an excess temperature and, thus, outputs a signal to the evaluation. This case can occur, for example, when respectively two temperature-protected high-side and low-side switches are interconnected to form a H-bridge and when a motor represents the load. Since the motor represents an inductance, reactance currents can activate the integrated reverse diode and produce free charge carriers.

In order to prevent this undesired condition, it is known to integrate the temperature sensor with a suitable, permanently implanted charge carrier diffusion that annularly surrounds the temperature sensor. The emitted charge carriers can be captured by applying a voltage between the charge carrier diffusion and the integrated reverse diode. As a result thereof, the temperature sensor is protected against the penetration of charge carriers. The charge carrier diffusion rings, which

are also referred to as "suction rings", however, have only a limited effect given high currents through the integrated reverse diode. In order also to be able to capture the charge carriers given high currents, the charge carrier diffusion would have to be implemented extremely broad. This, however, would have the disadvantageous effect that the temperature sensor exhibits a relatively great distance from the hottest location of the semiconductor switch element. It is precisely in semiconductor switches with a high current density, however, that the reaction time of the temperature sensor given thermal overload of the semiconductor switch element is of great significance. When, on the other hand, the charge carrier diffusion is implemented too low, this cannot adequately efficiently protect the temperature sensor given extremely high currents through the reverse diode D1 in order to prevent the undesired, parasitic effects to the temperature sensor.

Proceeding on the basis of this prior art, therefore, an object of the present invention is to provide a temperature-protected semiconductor switch that enables the response of the temperature sensor in a simple way only in case of an excess temperature.

SUMMARY OF THE INVENTION

In the temperature-protected semiconductor switch of the present invention, such object is achieved in that a charge carrier detector is provided which generates a second signal given the occurrence of free charge carriers in the semiconductor body.

The charge carrier detector is advantageously designed such that a parasitic component is formed between the charge carrier detector, the semiconductor body and at least one cell of the semiconductor switch element. When free charge carriers are produced, this parasitic structure enables the integrated reverse diode to generate a signal. When the first and second signals are supplied for evaluation and are logically operated with one another thereat, then the indication of an

unambiguous excess temperature in the semiconductor switch element is dependably produced.

In an embodiment, the charge carrier detector is arranged neighboring the temperature sensor which is, in turn, applied in the proximity of the hottest location of the semiconductor switch. Ideally, the charge carrier detector is arranged neighboring a signal line of the temperature sensor that leads out of the semiconductor switch. In this case, a signal line of the charge carrier detector can be conducted out of the semiconductor switch spatially adjacent to the signal line of the temperature sensor. A particularly simple layout of the semiconductor switch is thus possible since only a few modifications need be undertaken compared to a semiconductor switch known from the prior art.

In an embodiment, the evaluation means can be integrated together with the semiconductor switch, wherein it is monolithically integrated in the same semiconductor body. In this case, an advantageous space-arrangement of the temperature-protected semiconductor switch is possible. Of course, it is also conceivable to accommodate the evaluation means in a separate semiconductor chip and, for example, to apply this on the semiconductor switch with a chip-on-chip mounting.

Additional features and advantages of the present invention are described in, and will be apparent from, the Detailed Description of the Preferred Embodiments and the Drawings

DESCRIPTION OF THE DRAWINGS

Figure 1a shows a schematic plan view onto a temperature-protected semiconductor switch of the prior art;

Figure 1b shows the circuit diagram associated with the semiconductor switch of Figure 1a;

Figure 2 shows a schematic plan view onto the temperature-protected semiconductor switch of the present invention;

Figure 3 shows the electrical circuit diagram associated with the semiconductor switch of Figure 2; and

Figure 4 shows a cross section through the semiconductor body of the temperature-protected semiconductor switch of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 2 shows a schematic plan view onto the inventive, temperature-protected semiconductor switch 1. This is composed of a semiconductor switch element T1 that is, in turn, composed of a number of MOS cells (not shown) connected in parallel. A temperature sensor TS is attached in the proximity to the hottest location of the semiconductor switch element TS1, the temperature sensor TS outputting a signal via a signal line SL1 to a status output ST1 when a predetermined temperature threshold is upwardly exceeded. A charge carrier detector LD is arranged neighboring the temperature sensor TS, this detector LD likewise including a signal line SL2 that is connected to a status output ST2. The charge carrier detector LD is thereby arranged neighboring the temperature sensor TS, whereby the preferred location exists close to the junction of the signal line SL1 and the temperature sensor TS. The charge carrier detector LD, of course, could be arranged at any arbitrary location in the semiconductor switch element T1. The illustrated embodiment, however, represents the form that is simplest to produce.

Figure 3 shows the electrical circuit diagram of the inventive temperature-protected semiconductor switch 1. The semiconductor switch element T1 is implemented as a MOSFET that, due to technology, includes an integrated reverse diode D1. The anode of the reverse diode D1 is thereby connected to the source terminal of the MOSFET, whereas the cathode is in communication with the drain terminal. Further, the semiconductor switch 1 includes the temperature sensor TS and charge carrier detector LD, both of which are connected to an evaluation means AW via a signal line SL1 or, respectively, SL2. The evaluation means AW generates a signal at a status output ST3 that derives from an operation of the signals adjacent the status outputs ST1 or, respectively, ST2.

The evaluation means thereby works as follows. It is assumed that the temperature sensor TS generates a logical H in case a predetermined temperature is upwardly exceeded. When the integrated reverse diode D1 produces free charge carriers, then a logical H is adjacent the status output ST2; otherwise, a logical L is present.

When, due to a specific operating condition, the reverse diode D1 is operated in a flow direction, then it produces free charge carriers. As a result, the temperature sensor TS responds due to a parasitic structure and generates a logical H at the status output ST1. At the same time, the charge carrier detector LD also responds so that it likewise generates a logical H at its status output ST2. In this case, the evaluation means AW generates, for example, a logical L at its status output ST3, this being equivalent to a normal operating condition.

When, due to an abnormal operating condition, the semiconductor switch T1 becomes extremely hot, then the temperature sensor TS responds and generates a logical H at the status output ST1. Since, however, the reverse diode D1 does not produce any free charge carriers in this case, a logical L remains at the status output ST2. The evaluation means AW generates a logical H at its status output ST3 from these two input signals, this being equivalent to an excess temperature. In this case, a further evaluation means (not shown) can be activated which, for example, switches the semiconductor switch 1 off or, on the other hand, activates a current limitation.

Figure 4 shows a cross section through the semiconductor body of the temperature-protected semiconductor switch 1. In order to further illustrate the functionality of the present invention, the electrical circuit symbols also are entered. A number of MOS cells M are arranged in the semiconductor body. For the sake of simplicity, only a single such MOS cell M is shown in Figure 4. The MOS cells M, however, surround the temperature sensor TS and the charge carrier detector at all sides. The MOS cell M is arranged in a known way; i.e., a p-doped well 3 is let into the n-doped semiconductor body wherein a n-doped source zone

is, in turn, arranged in the well 3. The source zone 4 is thereby electrically externally connected to a source terminal. The gate electrodes G are arranged over the p-well via a gate oxide (not shown). The n-doped semiconductor body 2 is connected to a drain contact D.

A temperature sensor TS is arranged neighboring an MOS cell M. In the present figure, this is implemented as bipolar transistor 8. To this end, a p-well 5 is let into the semiconductor body 2, and a highly n-doped layer 6 is, in turn, placed in said p-well 5. The n-doped layer 6 is connected to the signal line SL1 with the status output ST1. The npn bipolar transistor 8 is formed by this structure.

The charge carrier detector LD is arranged neighboring the temperature sensor TS and is embodied in the form of a highly p-doped well in the semiconductor body 2. The p-doped well 7 is connected to the status output ST2 via the signal line SL2.

The p-well 3 together with the n-doped semiconductor body 2 forms the technologically caused reverse diode D1. When this diode D1 is temporarily operated in flow direction, i.e. from the p-well to the semiconductor body 2, then the parasitic bipolar transistor 9, which is formed of the p-well 3, the semiconductor body 2 and the p-well 5 of the temperature sensor become simultaneously active. When, consequently, charge carriers are released from the p-well 3 to the semiconductor body 2, then a current flows into the p-well 5 via the parasitic bipolar transistor 9. This represents the base of the temperature sensor TS implemented as a bipolar transistor which, thus, produces a signal at the status output ST1 that simulates a temperature rise. At the same time, however, the parasitic bipolar transistor 10 also becomes active, this being formed of the p-well 3 of the MOS cell M, of the semiconductor body 2 and of the p-well 7 of the charge carrier detector LD. A signal is therefore generated at the status output ST2. On the basis of the suitable operation of the signals adjacent the status outputs ST1 and ST2, a true excess temperature can be distinguished in the evaluation means AW from an apparent excess temperature.

As a result of this simple procedure, a very effective temperature monitoring system can be effected both in a very simple way and, above all else, in a space-saving fashion. As desired, the temperature sensor can be integrated in the proximity of the hottest location of the semiconductor switch 1. The disadvantages from the above-described prior art are thus avoided. The manufacture of the inventive, temperature-protected semiconductor switch is possible with only a few modified manufacturing steps compared to a standard, temperature-protected semiconductor switch.

Although the present invention has been described with reference to specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the spirit and scope of the invention as set forth in the hereafter appended claims.

I Claim as My Invention:

1. A temperature-protected semiconductor switch, comprising:

a semiconductor body of first conductivity type;

a semiconductor switch element formed of a plurality of cells connected in parallel and including an integrated reverse diode;

a temperature sensor which generates a first signal given the occurrence of an excess temperature, wherein the semiconductor switch element and the temperature sensor are integrated together in the semiconductor body; and

a charge carrier detector that generates a second signal given the occurrence of free charge carriers in the semiconductor body.

2. A temperature-protected semiconductor switch as claimed in claim 1, further comprising:

a parasitic component formed between the charge carrier detector, the semiconductor body and at least one cell of the semiconductor switch element.

3. A temperature-protected semiconductor switch as claimed in claim 1, further comprising:

an evaluation means, wherein the first and second signals are supplied to the evaluation means and logically operated with one another thereat for indicating an unambiguous excess temperature in the semiconductor switch element.

4. A temperature-protected semiconductor switch as claimed in claim 1, wherein the charge carrier detector is positioned adjacent the temperature sensor.

5. A temperature-protected semiconductor switch as claimed in claim 1, wherein the temperature sensor is attached proximate a hottest location of the semiconductor body.

6. A temperature-protected semiconductor switch as claimed in claim 1, wherein the charge carrier detector is positioned adjacent a signal line of the temperature sensor leading out of the semiconductor switch.

7. A temperature-protected semiconductor switch as claimed in claim 3, wherein the evaluation means is monolithically integrated with the semiconductor switch.

8. A temperature-protected semiconductor switch as claimed in claim 1, further comprising:

at least one of a bipolar transistor and a thyristor as the temperature sensor.

9. A temperature-protected semiconductor switch as claimed in claim 1, wherein the first conductivity type is n-conductive.

ABSTRACT OF THE DISCLOSURE

A temperature-protected semiconductor switch having a semiconductor switch element composed of a number of cells connected in parallel and an integrated reverse diode, and further having a temperature sensor wherein the semiconductor switch element and the temperature sensor are integrated together in a semiconductor body of a first conductivity type. Upon occurrence of an excess temperature, the temperature sensor generates a first signal. A charge carrier detector is also provided which generates a second signal given the occurrence of free charge carriers caused by the integrated reverse diode in the semiconductor body. The first and second signals are supplied to an evaluation means that, for example, undertakes the shut-off of the semiconductor switch only in the case of a true excess temperature.

FIG 1A

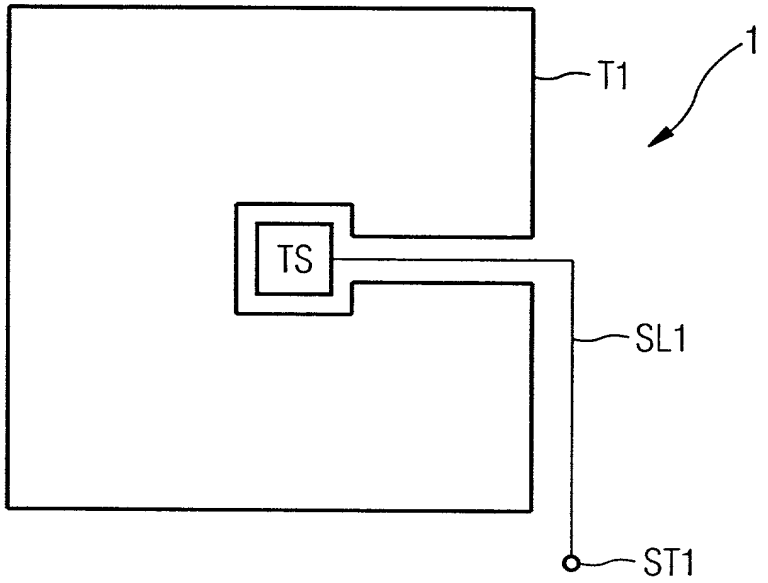


FIG 1B

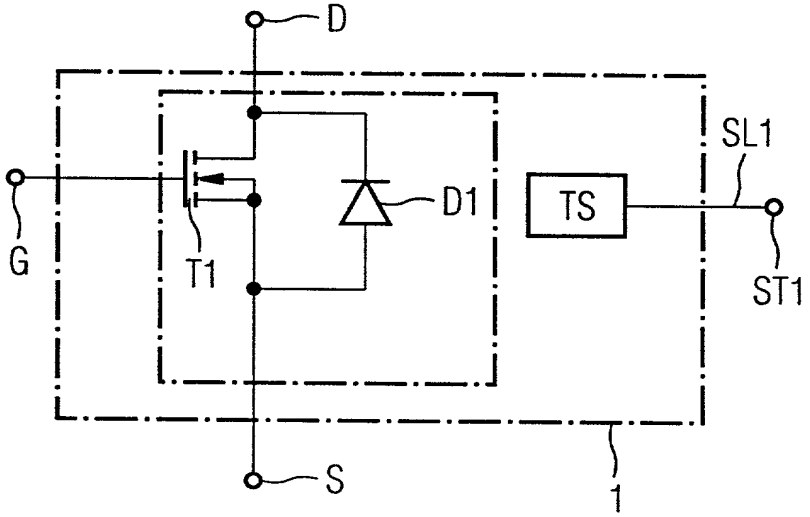


FIG 2

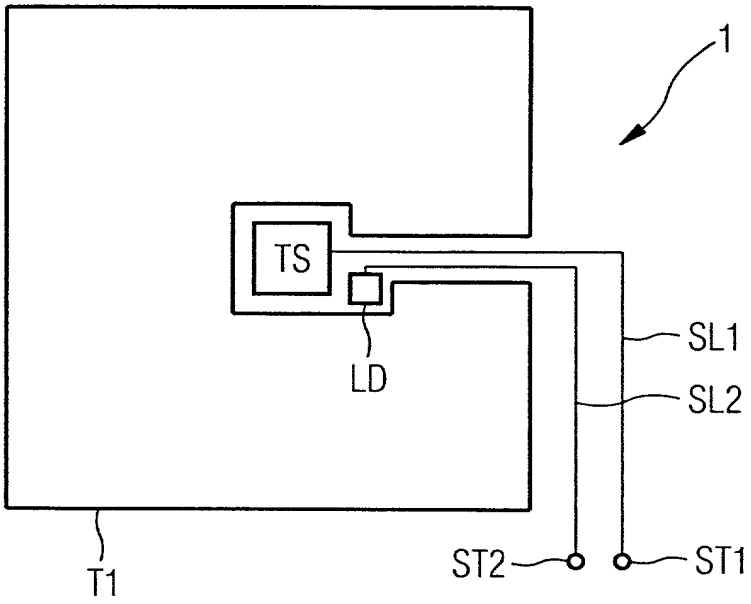
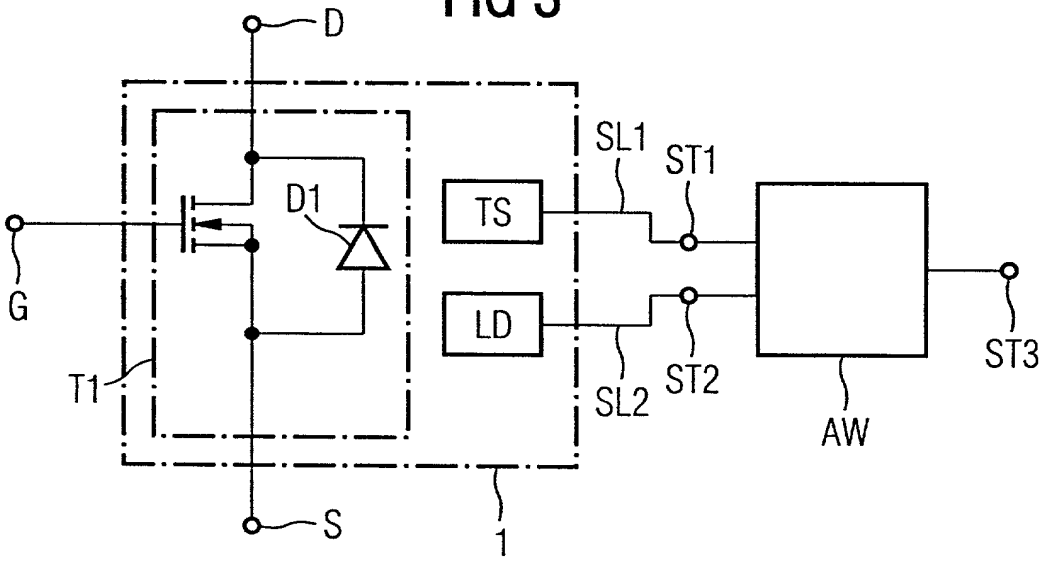


FIG 3



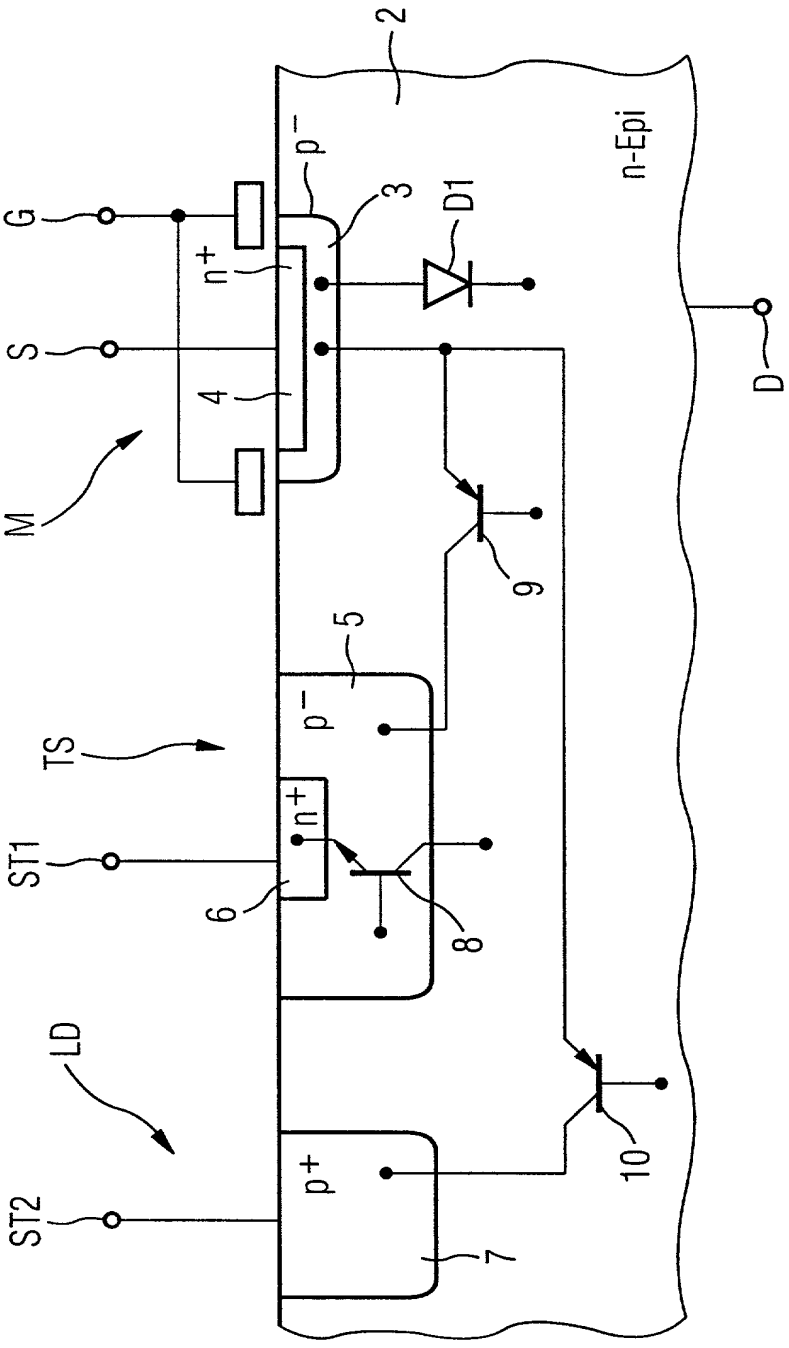


FIG 4

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DATA TRANSMISSION METHOD AND SYSTEM, PARTICULARLY IN AN OCCUPANT SAFETY SYSTEM IN A VEHICLE

Case No. **P00,0184**, the specification of which

(check one)
- X is attached hereto.
- ___ was filed on _____, as Application Serial No._____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent Office all information which is known to me to be material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, 1.56.[1]

I do not know and do not believe this invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and I believe that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as identified below:

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below

Prior Foreign Application(s) Number	Country	Date
199 04 575.5	**Germany**	**February 4, 1999**

and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the above listed application on which priority is claimed:

Prior Foreign Application(s) Number	Country	Date

---

[1] (b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a *prima facie* case of unpatentability of a claim, or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A *prima facie* case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

If no priority is claimed, I have identified all foreign patent applications filed prior to this application:
Prior Foreign Application(s)
Number Country Date

And I hereby appoint Messrs. John D. Simpson (Registration No. 19,842), Dennis A. Gross (24,410), Robert M. Barrett, (30,142), Steven H. Noll (28,982), Kevin W. Guynn (29,927), Robert M. Ward (26,517), Brett A. Valiquet (27,841), Edward A. Lehman (22,312), David R. Metzger (32,919), Todd S. Parkhurst (26,517), James D. Hobart (24,149), Melvin A. Robinson (31,870), Joseph P. Reagen (35,322), Michael R. Hull (35,902), Michael S. Leonard (37,557), William E. Vaughan (39,056) and Lewis T. Steadman (17,074), all members of the firm of Hill & Simpson, A Professional Corporation

Telephone: 312/876-0200 Ext. 3491

my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and direct that all correspondence be forwarded to:

Hill & Simpson
A Professional Corporation
85th Floor Sears Tower, Chicago, Illinois 60606

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor **RAINALD SANDER**

Inventor's signature _____ Date _____
Residence 81543 Muenchen, Germany
Citizenship Germany
Post Office Address Alemannenstr. 8
81543 Muenchen, Germany

Full name of second joint inventor,
(if any) _____

Inventor's signature _____ Date _____
Residence _____
Citizenship _____
Post Office Address _____

Full name of third joint inventor,
(if any) _____

Inventor's signature _____ Date _____
Residence _____
Citizenship _____
Post Office Address _____